Memory Module Data Sheet

ADQYE1A08
DDR2-1066+(CL5) 240-Pin EPP U-DIMM
1GB (128M x 64-bits)

General Description：

The ADATA's **ADQYE1A08** is a 128Mx64 bits 1GB(1024MB) DDR2-1066(CL5) SDRAM EPP memory module, The SPD is programmed to JEDEC standard latency 800Mbps timing of 5-5-5-18 at 1.8V. The module is composed of eight 128Mx8 bits CMOS DDR2 SDRAMs in FBGA package and one 2Kbit EEPROM in 8pin TSSOP (TSOP) package on a 240pin glass–epoxy printed circuit board.

The **ADQYE1A08** is a Dual In-line Memory Module and intended for mounting onto 240-pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features：

• Power supply(Normal): VDD & VDDQ = 1.8V ± 0.1V
• 1.8V (SSTL_18 compatible) I/O
• EPP (Enhanced Performance Profiles) support
• Timing Reference
  - DDR2 800 CL5-5-5-18 at 1.8V
  - DDR2 800 CL4-4-4-12 at 2.0V (EPP Profile 1)
  - DDR2 1066 CL5-5-5-15 at 2.3V (EPP Profile 2)
• Burst Length: 4, 8
• Programmable Additive Latency: 0, 1, 2, 3, 4
• Bi-directional, differential data strobe (DQS and /DQS)
• Differential clock input (CK, /CK) operation
• DLL aligns DQ and DQS transition with CK transition
• Double-data-rate architecture.
• Auto & Self refresh
• Average Refresh period 7.8μs
• Off-Chip Driver (OCD) Impedance Adjustment
• On Die Termination (ODT)
• Lead-free products are RoHS compliant
• EEPROM VDDSPD=3.3V (Typical)
• PCB Height 30.00mm (1.181”), Single sided component
• Clock Cycle Time (tCK):
  - DDR2-800 tCK=2.5ns
  - DDR2-1066 tCK=1.875ns
• Refresh to Active/Refresh Command Time (tRFC): 127.5ns

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Pin Assignment：

Pin	Front	Pin	Front	Pin	Front		Pin	Back	Pin	Back	Pin	Back
1	VREF	41	VSS	81	DQ33		121	VSS	161	NC , CB4	201	VSS
2	VSS	42	NC , CB0	82	VSS		122	DQ4	162	NC , CB5	202	DM4
3	DQ0	43	NC , CB1	83	/DQS4		123	DQ5	163	VSS	203	NC
4	DQ1	44	VSS	84	DQS4		124	VSS	164	NC , DM8	204	VSS
5	VSS	45	NC , /DQS8	85	VSS		125	DM0	165	NC	205	DQ38
6	/DQS0	46	NC , DQS8	86	DQ34		126	NC	166	VSS	206	DQ39
7	DQS0	47	VSS	87	DQ35		127	VSS	167	NC , CB6	207	VSS
8	VSS	48	NC/CB2	88	VSS		128	DQ6	168	NC , CB7	208	DQ44
9	DQ2	49	NC/CB3	89	DQ40		129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41		130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS		131	DQ12	171	CKE1	211	DM5
12	DQ8	52	CKE0	92	/DQS5		132	DQ13	172	VDD	212	NC
13	DQ9	53	VDD	93	DQS5		133	VSS	173	A15	213	VSS
14	VSS	54	BA2	94	VSS		134	DM1	174	A14	214	DQ46
15	/DQS1	55	NC	95	DQ42		135	NC	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43		136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS		137	CK1	177	A9	217	DQ52
18	NC	58	A7	98	DQ48		138	/CK1	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49		139	VSS	179	A8	219	VSS
20	VSS	60	A5	100	VSS		140	DQ14	180	A6	220	CK2
21	DQ10	61	A4	101	SA2		141	DQ15	181	VDDQ	221	/CK2
22	DQ11	62	VDDQ	102	NC , TEST		142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS		143	DQ20	183	A1	223	DM6
24	DQ16	64	VDD	104	/DQS6		144	DQ21	184	VDD	224	NC
25	DQ17	65	VSS	105	DQS6		145	VSS	185	CK0	225	VSS
26	VSS	66	VSS	106	VSS		146	DM2	186	/CK0	226	DQ54
27	/DQS2	67	VDD	107	DQ50		147	NC	187	VDD	227	DQ55
28	DQS2	68	NC	108	DQ51		148	VSS	188	A0	228	VSS
29	VSS	69	VDD	109	VSS		149	DQ22	189	VDD	229	DQ60
30	DQ18	70	A10/AP	110	DQ56		150	DQ23	190	BA1	230	DQ61
31	DQ19	71	BA0	111	DQ57		151	VSS	191	VDDQ	231	VSS
32	VSS	72	VDDQ	112	VSS		152	DQ28	192	/RAS	232	DM7
33	DQ24	73	/WE	113	/DQS7		153	DQ29	193	/S0	233	NC
34	DQ25	74	/CAS	114	DQS7		154	VSS	194	VDDQ	234	VSS
35	VSS	75	VDDQ	115	VSS		155	DM3	195	ODT0	235	DQ62
36	/DQS3	76	/S1	116	DQ58		156	NC	196	A13	236	DQ63
37	DQS3	77	ODT1	117	DQ59		157	VSS	197	VDD	237	VSS
38	VSS	78	VDDQ	118	VSS		158	DQ30	198	VSS	238	VDDSPD
39	DQ26	79	VSS	119	SDA		159	DQ31	199	DQ36	239	SA0
40	DQ27	80	DQ32	120	SCL		160	VSS	200	DQ37	240	SA1

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Pin Description：

PIN	NAME	FUNCTION
CK0~CK2, /CK0~/CK2	System Clock	Active on the positive and negative edge to sample all inputs.
CKE0	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/S0	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
A0~A13	Address	Row / Column address are multiplexed on the same pins. (Row Address：A0~A13 , Column Address：:A0~A9 , Auto precharge：A10/AP)
BA0~BA2	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ63	Data	Data and check bit inputs / outputs are multiplexed on the same pins.
DQS0~DQS7, /DQS0~/DQS7	Data Strobe	Bi-directional Data Strobe
DM0~DM7	Data Mask	Mask input data when DM is high.
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
VDD / VSS	Power Supply/Ground	Power and Ground for the input buffers and the core logic.
VREF	Power Supply reference	Power Supply for reference
VDDSPD	SPD Power Supply	Serial EEPROM power Supply
SDA	Serial data I/O	EEPROM serial data I/O
SCL	Serial clock	EEPROM clock input
SA0~SA2	Address in EEPROM	EEPROM address input
ODT0	On Die Termination	When high, termination resistance is enabled for all DQ, /DQ and DM pins, assuming the function is enabled in the Extended Mode Register Set.
NC	No Connection	This pin is recommended to be left No Connection on the device.

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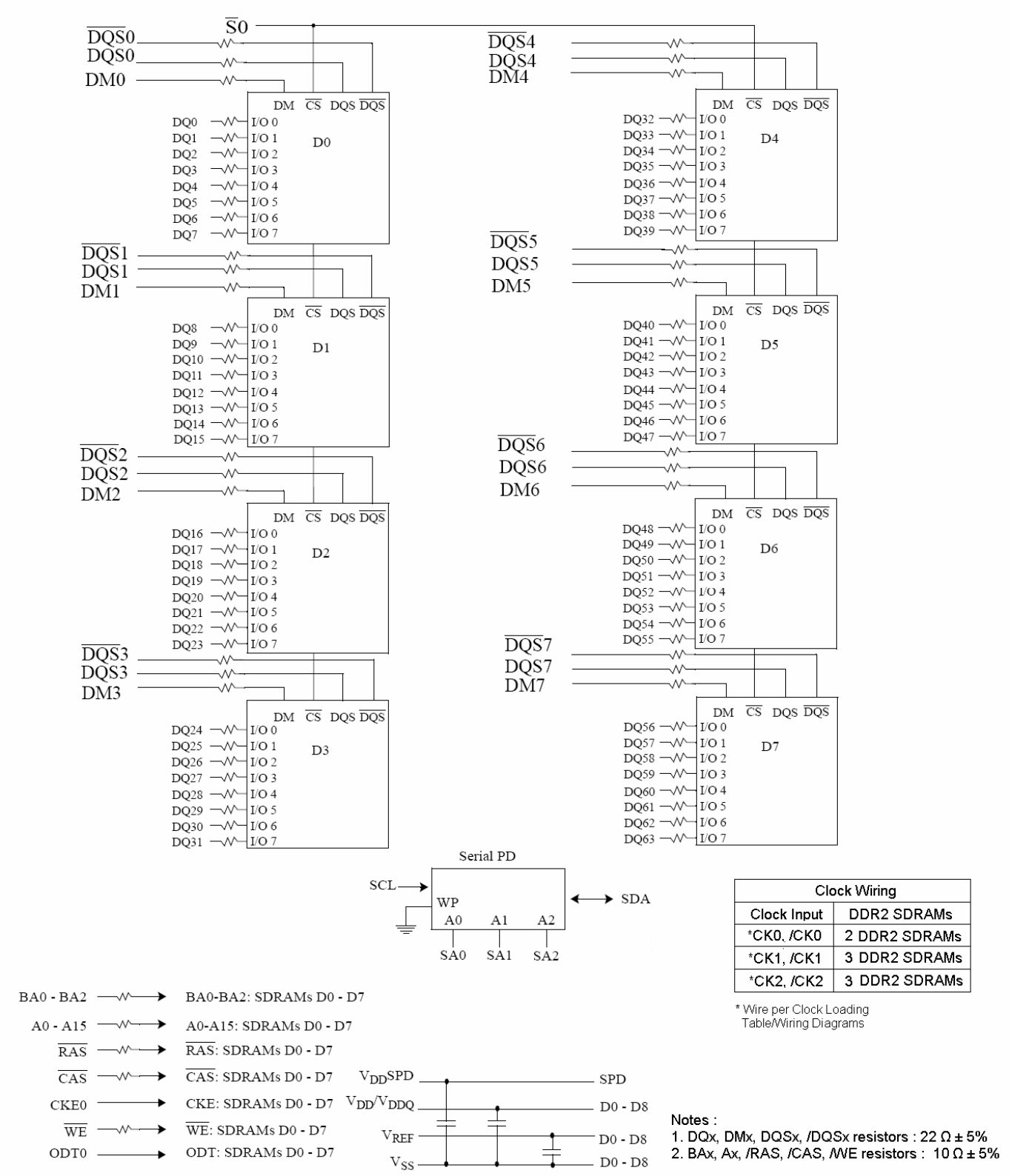
Block Diagram：



Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0, /CK0	2 DDR2 SDRAMs
*CK1, /CK1	3 DDR2 SDRAMs
*CK2, /CK2	3 DDR2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes :
1. DQx, DMx, DQSx, /DQSx resistors : 22 Ω ± 5%
2. BAx, Ax, /RAS, /CAS, /WE resistors : 10 Ω ± 5%

Absolute Maximum Ratings：

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	V_{DD}	-1.0 ~ +2.3	V
Voltage on VDDQ supply relative to Vss	V_{DDQ}	-0.5 ~ +2.3	V
Voltage on VDDL supply relative to Vss	V_{DDQ}	-0.5 ~ +2.3	V
Voltage on any pin relative to Vss	V_{IN}, V_{out}	-0.5 ~ +2.3	V
Storage temperature	T_{STG}	-55 ~ +100	℃

Note: DDR2 SDRAM component specification.

Operation Temperature Condition

Parameter	Symbol	Value	Unit	Note
DRAM Component Case Temperature Range	TC	0~+95	℃	1

Note: (1) If the DRAM case temperature is above 85'C, the Auto-Refresh command interval has to be reduced to tREFI=3.9us.

DC Operating Condition：

Voltage referenced to Vss = 0V, VDD&VDDQ=1.8V±0.1V, T_C = 0 to 85 ℃

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	1.7	1.9	V	4,5
	V_{DDSPD}	1.7	3.6	V	
Supply Voltage for DLL	V_{DDL}	1.7	1.9	V	4
Supply Voltage for Output	V_{DDQ}	1.7	1.9	V	4,5
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1,2
Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	3

Note: (1) There is no specific device VDD supply voltage requirement for SSTL_1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

(2) The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically, the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

(3) Peak to peak ac noise on VREF may not exceed +/- 2% VREF (ac).

(4) VTT of transmitting device must track VREF of receiving device.

(5) VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together.

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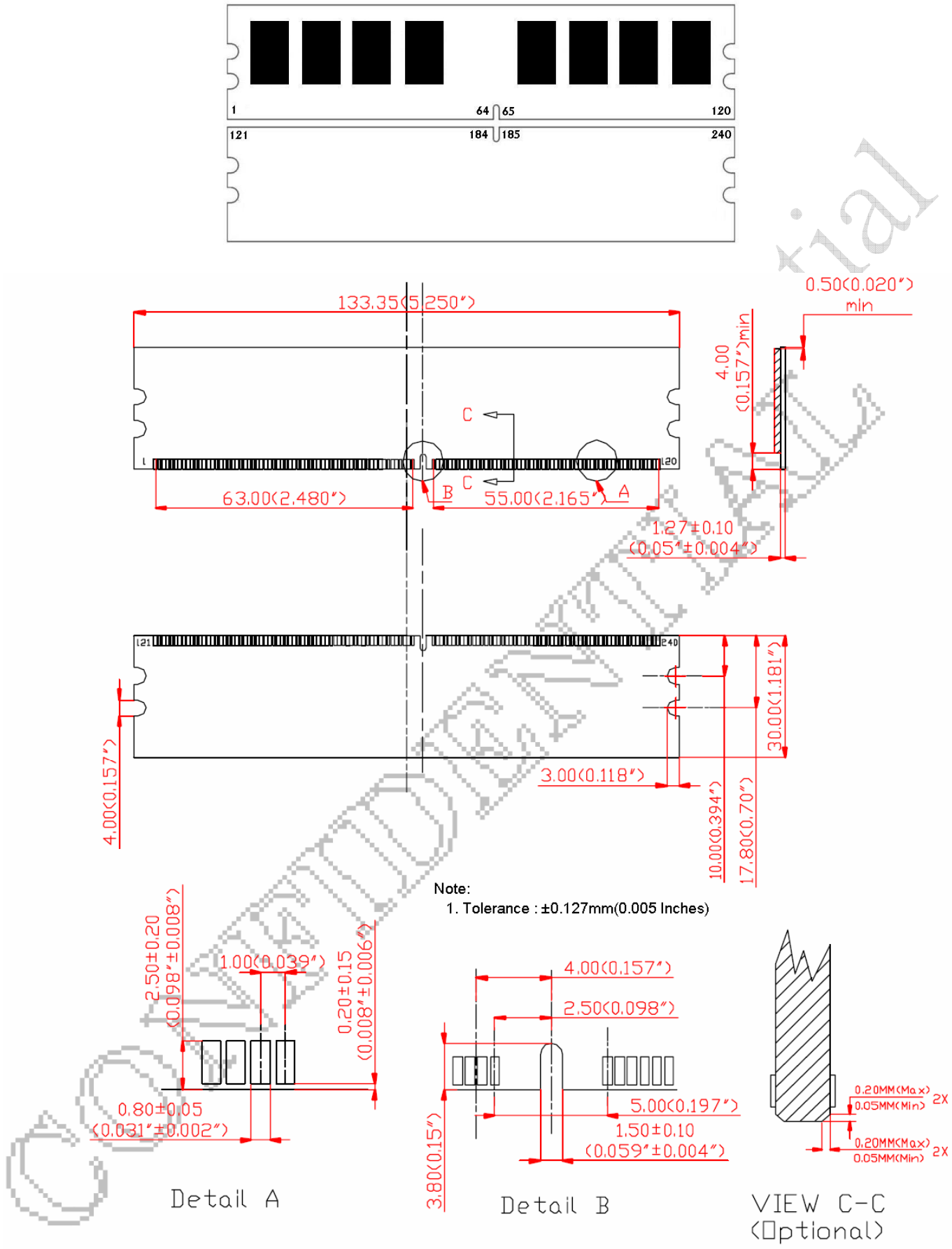
Package Dimensions：



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